REMARKS

Claims 1-70 are pending in the application. The Applicants' attorney has amended claims 5-7, 22-23, 28-29, 46-48, 57 and 62. In view of the following, it is respectfully submitted that all of the currently unallowed claims are in condition for allowance.

Objection to the Drawings

The drawings stand objected to for allegedly failing to show a "processor" as recited in claim 9. FIG. 4 of the present application is a block diagram of a pixel circuit 100 according to an embodiment of the invention. Referring to page 16, lines 5-6, the present application discloses that "the pixel circuit 100 may be a processor . . . ." As such, the drawings clearly illustrate a processor. Accordingly, the Applicants' attorney respectfully requests the Examiner to withdraw the objection to the drawings.

Rejection of Claims 39-44 Under 35 U.S.C. § 112, First Paragraph

Claim 39

Claim 39 recites "an image buffer having a first input terminal coupled to the second pixel-value output terminal and having a second input terminal coupled to the combiner output terminal."

The Examiner states that, because Applicants' FIG. 4 illustrates the output of the combiner 106 being input to a clipper circuit 124 rather than the image buffer 110, claim 39 is not enabling. However, as shown in FIG. 4 and discussed at page 11, lines 19-27 of the specification, the clipper circuit 124 receives dark pixel values from the combiner 106 and then provides modified pixel values to an input 128 of the image buffer 110. Therefore, the input 128 of the image buffer 110 is "coupled" to the output of the combiner 106. The scope of this claim is intended to cover an embodiment in which the clipper circuit 124 is omitted. As such, the Applicants' attorney respectfully submits that the specification clearly enables the subject matter of claim 39.

Claims 40-44

Claims 40-44 are patentable by virtue of their dependency from claim 39.

Rejection of Claims 5-7, 20-23, 46-47 and 57 Under 35 U.S.C. § 112, Second Paragraph

Claims 5-7, 20-22 and 46

Claims 5-7 and 46 have been amended by Applicants' attorney and are now in condition for allowance.

Claim 15, from which claims 20-22 depend, recites adding a first compensation value to a first pixel value and adding a second compensation value to a second pixel value. Accordingly, each limitation of claims 20-22 has antecedent basis, and the Examiner is respectfully requested to withdraw his rejection of claims 20-22 on this ground.

Claims 6, 22 and 47

Claims 6, 22 and 47 have been amended by Applicants' attorney and are now in condition for allowance.

Claim 23

Claim 23 has been amended by Applicants' attorney and is now in condition for allowance.

Claim 57

Claim 57 has been amended by Applicants' attorney and is now in condition for allowance.

Rejection of Claims 1-3, 5, 8-17, 20, 23-25, 30-31, 33-38, 45-46, 48-54, 56, 58-59, 63 and 65-70 Under 35 U.S.C. § 102 As Being Anticipated By US Patent No. 5,436,736 to Shono

Claims 1 and 45

Claims 1 and 45 each recite modifying a pixel value if the pixel value has a predetermined relationship to a threshold value.

For example, referring, *e.g.*, to FIGS. 4-5 and page 10, line 32 – page 11, line 15 of the present application, a circuit 100 includes a threshold comparator circuit 102, which compares pixel values of each pixel in an image to a respective threshold value. The circuit 102 provides the pixel values that are below the threshold value to a combiner 106. A random-number generator 112 generates a respective random number for each of these pixel values. The generator 112 provides the random numbers to the combiner 106. Thus, for each of these pixel values, the generator 112 provides a respective random number to the combiner 106, which combines the random number with a respective pixel value to generate a modified pixel value.

Shono, on the other hand, fails to teach or suggest modifying a pixel value if such value has a predetermined relationship to a threshold value. Shono, at, e.g., FIG. 4 and col. 5, lines 55-65, teaches an operator 25 that divides input pixel data into higher-order bit data and lower-order bit data. The operator 25 sends the higher-order bit data to an adder 22 and the lower-order bit data to a comparator 23. The comparator 23 compares a threshold value output from a random number generator 24 with the lower-order bit data and binarizes the lower-order bit data in accordance with the comparison result. The adder 22 adds the higher-order bit data to the binarized data.

The Examiner cites the adder 22 as modifying a pixel value if the pixel value has a predetermined relationship to a threshold value. However, Shono fails to teach that the adder 22 in any way qualifiedly adds the data. That is, the binarized data is combined with the higher-order bit data (*i.e.*, modified) irrespective of any precondition (*e.g.*, a threshold value relationship, as claimed).

Claims 15, 24, 31, 54, 58 and 63

Claims 15, 24, 31, 54, 58 and 63 are patentable for reasons similar to those discussed above in connection with claims 1 and 45.

Claims 2-3, 5, 8-10, 16-17, 20, 23, 25, 30, 33, 46, 48-50, 56, 59 and 65

Claims 2-3, 5, 8-10, 16-17, 20, 23, 25, 30, 33, 46, 48-50, 56, 59 and 65 are patentable by virtue of their respective dependencies from claims 1, 15, 24, 31, 45, 54, 58 and 63.

Claims 11, 24, 31, 34, 51, 58, 63 and 66

Claims 11, 24, 31, 34, 51, 58, 63 and 66 each recite combining/adding a random number with/to a pixel value.

For example, referring, *e.g.*, to FIGS. 4-5 and page 10, line 32 – page 11, line 15 of the present application, a circuit 100 includes a threshold comparator circuit 102, which compares pixel values of each pixel in an image to a respective threshold value. The circuit 102 provides the pixel values that are below the threshold value to a combiner 106. A random-number generator 112 generates a respective random number for each of these pixel values. The generator 112 provides the random numbers to the combiner 106. Thus, for each of these pixel values, the generator 112 provides a respective random number to the combiner 106, which combines the random number with a respective pixel value to generate a modified pixel value.

Shono, on the other hand, fails to teach or suggest a random number and pixel value being combined or added to one another. Shono, at, e.g., FIG. 4 and col. 5, lines 55-65, teaches an operator 25 that divides input pixel data into higher-order bit data and lower-order bit data. The operator 25 sends the higher-order bit data to an adder 22 and the lower-order bit data to a comparator 23. The comparator 23 compares a threshold value output from a random number generator 24 with the lower-order bit data and binarizes the lower-order bit data in accordance with the comparison result. The adder 22 adds the higher-order bit data to the binarized data. Shono fails to teach in

any way that the adder 22 receives a random number from the generator 24 or elsewhere, much less adds such a number to the bit data.

Claims 12-14, 25, 30, 33, 35-38, 52-53, 59, 65 and 67-70

Claims 12-14, 16-17, 20, 23, 25, 30, 33, 35-38, 52-53, 56, 59, 65 and 67-70 are patentable by virtue of their respective dependencies from claims 11, 24, 31, 34, 51, 58, 63 and 66.

Rejection of Claims 4, 6, 7, 18, 19, 21, 22, 26, 27, 32, 55, 60-61 and 64 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Shono

Claims 4, 6, 7, 18, 19, 21, 22, 26, 27, 32, 55, 60-61 and 64 are patentable by virtue of their respective dependencies from claims 1, 15, 24, 31, 54, 58 and 63.

CONCLUSION

The present patent application is in condition for allowance, and favorable consideration and a Notice of Allowance are respectfully requested. The Examiner is requested to contact the undersigned at the number listed below for a telephone interview if, upon consideration of this response, the Examiner determines any pending claims are not in condition for allowance.

In the event additional fees are due as a result of this Response, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

Respectfully submitted,
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